IN THE SPECIFICATION

Please amend the specification as follows.

Please amend paragraph [0377] as follows:

"[0377] Referring now to FIG. 34, a detailed block diagram of an exemplary embodiment of the collar logic block 2713 for each memory cluster 2710 is illustrated. The collar logic 2713 includes a controller 3410, a plurality of input receivers 3418 and a plurality of tristate bus drivers 3419. FIG. 34 illustrates four input receivers 3418A-3418D and four tristate bus drivers 3419 corresponding to the reconfigurable memory of FIG. 30. The input receivers 3418A-3418D receive data off of the cluster data bus input CLiDBIN 2718m and couple it into the respective input of a memory block on one of DATAINn buses 3718n. The input receivers 3418A-3418D are each respectively enabled by a separate input enable signal IENn respectively labeled IENA, IENB, IENC, and IEND in FIG. 34. The tristate bus drivers 3419A-3419D receive data output from the output latches of the memory blocks on the DATA OUTn buses 3719n. One of the tristate bus drivers 3419A-3419D selectively drives the cluster output data bus CliDBOUT 2719m. The tristate bus drivers 3419A-3419D are each respectively enabled by a separate output enable signal OENn respectively labeled OENA, OENB, OENC, and OEND in FIG. 34. In one embodiment of the invention, the plurality of tristate bus drivers 3419 form an output multiplexer in the collar logic 2713 of each memory cluster 2710."